A Low Power and Low Noise Frequency Synthesizer with a Integrated Quadrature VCO

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Abstract — **A frequency synthesizer including a integrated quadrature VCO and a few novel circuits is presented in a 0.18um CMOS technology. A 16/17 dual modulus prescaler operates up to 5.1GHz due to the fast (about 10GHz) operation of the proposed complementary clocking (CC) dynamic flip-flop. Also, a phase frequency detector (PFD) utilizing the charge pump current feedback, generates low spurious tones irrespective of the temperature or supply variations. The measured reference spur is less than -120dBc with a second order loop-filter of which bandwidth equals $f_{REF}/50$. The measured out- and in-band phase noise of the quadrature VCO is -140dBc@8MHz and -82dBc@10kHz, respectively. With a 1.8V power supply, the current consumption of the overall frequency synthesizer is only 7.5mA except 50Ω driving buffers.**

I. Introduction

The primary goal of frequency synthesizers in modern communication systems is providing a tunable local oscillator (LO) signal to frequency conversion mixers. The essential requirements of frequency synthesizers include high speed operation, low phase noise, good spurious performance, wide tuning range, and low power consumption. Generally, frequency synthesizers are composed of several circuits in phase locked loop (PLL). Among the circuits, prescaler, phase frequency detector (PFD), charge pump, and voltage controlled oscillator (VCO) dominate the above performances.

In a few GHz operating prescaler, common source logic (CSL) is more popular than true single phase clocking (TSPC) because the former has higher speed and less noise than the latter. But, the technology evolution enforces dynamic circuits to be used in a few GHz range because they have the merit of no static power consumption. Thus, most previous works were focused to enhance the speed of the flip-flops and have developed several circuits. However, the reported maximum speed of conventional TSPC prescaler is about 2-3GHz [1]-[3].

The dead-zone free PFD scheme usually inserts a delay in reset path of the flip-flop and generates simultaneous up/down pulse interval. This delay has to satisfy the time interval required to turn on and off the charge pump current. But this delay generates the spurious tones at the VCO output because of the charge-pump up/down current mismatch [4], [5]. Thus, the trade-off between dead-zone and the spurious level must be considered.

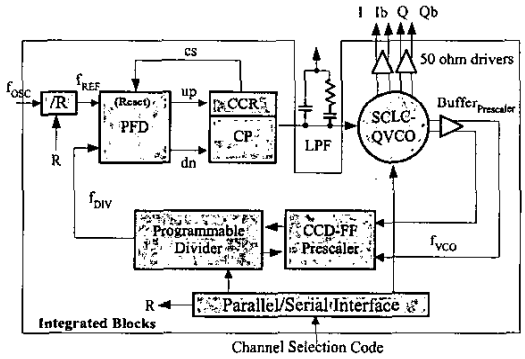

Fig. 1. Implemented frequency synthesizer

In this paper, therefore, we present a frequency synthesizer with an integrated quadrature VCO, which has several improved circuits compared with the previous works. Figure 1 shows the presented frequency synthesizer composed of the programmable reference counter (/R), phase frequency detector (PFD), current cell replica-charge pump (CCR-CP), low pass filter (LPF), switched capacitor LC-quadrature voltage controlled oscillator (SCLC-QVCO), complementary clocking dynamic flip flop prescaler (CCD-FF Prescaler), programmable divider, and parallel/serial interface.

II. The Frequency Synthesizer Design and Implementation

A. The prescaler design using the CC (Complementary Clocking) dynamic flip-flop

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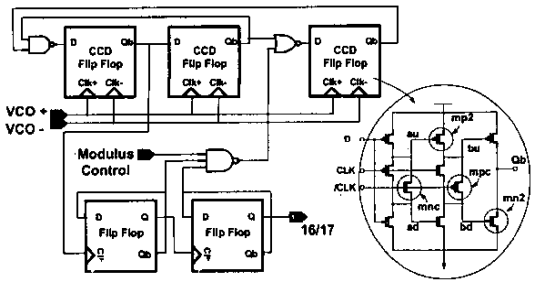


Fig. 2. Prescaler using the proposed CCD flip-flop

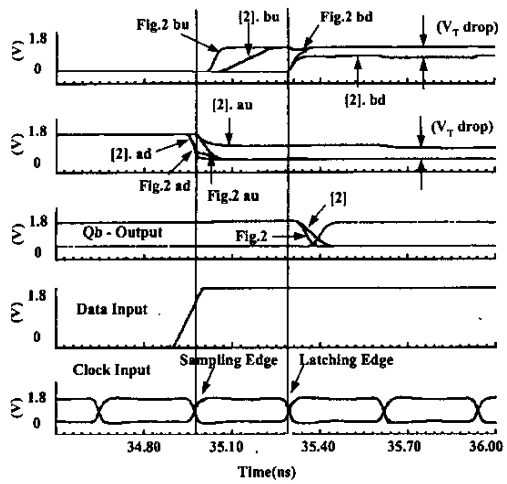
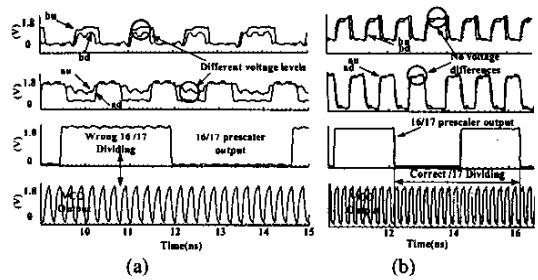


Fig. 3. Simulation results of the flip-flops

The TSPC flip-flop of [2] has minimum input transistor size and thus it can operate at higher input frequency than any other TSPC schemes. When charge sharing occurs, however, it has the critical problem of low driving capability caused by Vgs drop (near to V_T) of clock input transistor. So the next transistor becomes driven with reduced voltage (Vdd-V_T). This problem makes the flip-flop be in a low speed operation. Moreover, additional inverter stage lowering the speed is necessary to obtain Q output required for stable operation in cascade connection.

In order to enhance the operating speed and to reduce the clocking noise of the TSPC, we present the dual modulus prescaler using the complementary clocking dynamic flip-flop shown in Figure 2. Despite of the simple idea of using complementary clock signal, the proposed flip-flop has a good performance enough to doubling the maximum operation frequency compared with the previous one. The proposed flip-flop has complementary clock signal and additional *mnc* and *mpc* transistors to the conventional one. By employing this structure, there are



(0.18um/1.8V)	[2], Q-out	[2], Qb-out	Proposed
Toggle-flip flop		6 GHz	10 GHz
Prescaler(16/17)	1.9 GHz	3.4 GHz	5.1 GHz

(C)

Fig. 4. Waveforms of the conventional and the proposed circuit and maximum operating frequency
(a) Prescaler of the conventional flip-flop@4GHz, [2]
(b) Prescaler of the CCD flip-flop@4GHz
(c) Simulated maximum operating frequency

no voltage differences between *au* and *ad* node, *bu* and *bd* node during the turned-on interval of clock input transistors. This scheme makes *au* and *bd* nodes become fully high or fully low, and thus enhances the current driving capability of *mp2* and *mn2* transistors.

Figure 3 shows the simulated comparisons of the conventional [2] and the proposed flip-flop. When the input data 'H' is sampled, *bu* and *ad* nodes settle more rapidly, and the output of Qb is also faster in the proposed one. So, there is no problem to drive the next stage. In addition, the prescaler with the proposed flip-flop has less clock noise than the prescaler with conventional one, which is well shown in the simulated waveforms in Figure 4. The fast settling time and the drivability for the next stage of the proposed flip-flop stably enhances the speed of the designed prescaler shown in Figure 2. Finally, the maximum operating frequencies of the flip-flops and the prescalers are summarized in a table shown in Figure 4. The maximum operating frequency of the prescaler using the proposed flip-flop is about 5.1GHz.

B. PFD and CP design using the current sensing scheme

As mentioned previously, the reset delay in PFD must be minimized to reduce spur level on the condition of guaranteeing the switching time interval of the charge pump current.

Figure 5 shows the proposed PFD and the current cell replica-charge pump (CCR-CP) scheme to minimize the spurious level and resolve the dead-zone problem. The transistors of *mp1*, *mp2*, *mn1*, and *mn2* are the replica of the current cell of the charge pump supplying the up/down

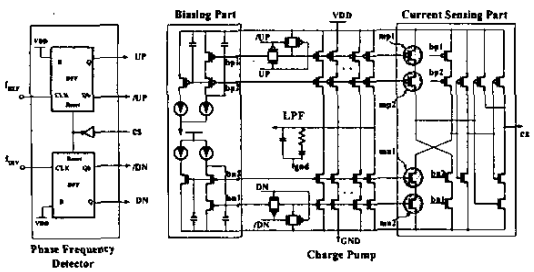


Fig. 5. Dead-Zone free PFD/CP using the charge pump current sensing

current to the loop filter. In the proposed scheme, when the simultaneous up/down current occurs, the current sensing (CS) signal feedbacks to the reset input of the PFD. Therefore, the minimum delay for reducing the spur level and for resolving the dead-zone problem is automatically detected in the proposed circuit scheme. In addition, this minimum delay is auto-detected and insensitive to the variation of the supply voltage, the temperature, and other parasitic effects.

C. Quadrature VCO design

The key characteristics of VCO design are adjusting the center frequency, tuning the frequency in a wide range, and minimizing the phase noise. The phase noise of the passive LC-tuned VCO can be expressed by the Leeson's equation for the white noise and the noise factor of [6] in the current limited regime [7].

$$L(\omega_m)_{SSB} = kT \frac{(1+\frac{4\gamma RI}{\pi V_o}+\gamma\frac{4}{9}g_{mcs}R)\cdot\omega_o LQ}{(\frac{4}{\pi}\omega_o LQI)^2\cdot Q^2}\cdot(\frac{\omega_o}{\omega_m})^2$$

$$= kT\frac{1}{\omega_o LQ^3}\cdot\frac{\pi^2(1+\gamma)}{16I^2}\cdot(\frac{\omega_o}{\omega_m})^2$$

, neglecting the current source noise

From this equation, we can design the passive LC-tuned VCO to have the required phase noise and the minimized current consumption assuming that the Q of the LC-tank is sufficiently high.

Figure 6 shows the implemented VCO and the measured frequency tuning range. The quadrature VCO for four phase outputs is realized by combining a couple of LC-tuned resonant oscillators. The each oscillator includes binary switched MIM capacitors for coarse tuning, a MOS varactor for fine tuning by the PLL operation, and NMOS/PMOS cross-coupled negative gm pairs for low current consumption. We use a rectangular symmetric

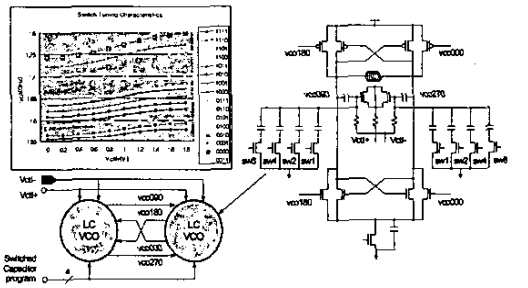


Fig. 6. Integrated quadrature VCO and measured switched tuning frequency

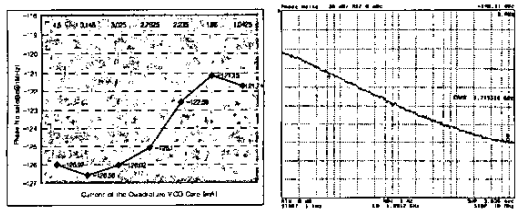
inductor having a 2um thickness Al-Cu metal top layer, and the quality factor is about 4.2@2GHz. The varactor is NMOS type, and the unit size of a gate finger is 0.5um x 5um (L x W). The size of the negative gm transistors is optimized to satisfy the oscillation condition, the frequency tuning, and the phase noise. The VCO frequency is tuned by the combination of the two methods, one is to use a small varactor in direct continuous control and the other is to use multiple MIM capacitors which are connected or disconnected to the resonant tank by the programmed binary switches (*sw1, sw2, sw4, sw8*). The small capacitance of the NMOS varactor is required for lowering the VCO gain and for minimizing the frequency variation resulting from other parasitic effects. In the other hand, it is also desirable that the varactor capacitance must not be too small to cover the frequency variation caused by process variation.

III. Experimental Results

Fig. 6 shows the measured frequency tuning range of the VCO from 1.55 GHz to 1.8 GHz by the varactor and switched tuning. The VCO gain by the varactor tuning is about 35MHz/V. The measured phase noise versus current consumption of the VCO is shown in Fig. 7(a), which can be expected from the equation in section II-C. Fig. 7(b) shows the measured phase noise of the free running VCO. The maximum phase noise is about -126.5dBc@1MHz and -140dBc@8MHz.

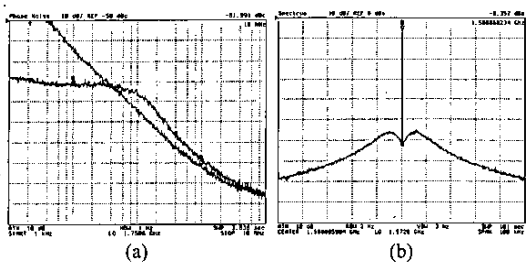
We experiment the frequency synthesizer using an external passive second-order low pass filter on the condition of 100kHz bandwidth, 5MHz f_{REF}, and 2.5mA VCO current shown in Fig. 7(a).

Fig. 8(a) shows the phase noise in both locked and free running state. Fig. 8(b) shows the spectrum in locked state of the frequency synthesizer. The in-band noise is about -82dBc@10kHz. The reference spur level is less than -120dBc at 50/f_{REF} loop filter bandwidth.



(a) (b)

Fig. 7. Measured characteristics of the free running VCO
(a) Phase noise vs current of the VCO core
(b) Measured phase noise



(a) (b)

Fig. 8. Measured characteristics of the locked state
(a) Phase noise of the locked state and the free running state (f_p=100kHz)
(b) Spectrum of the locked state (f_p=7kHz)

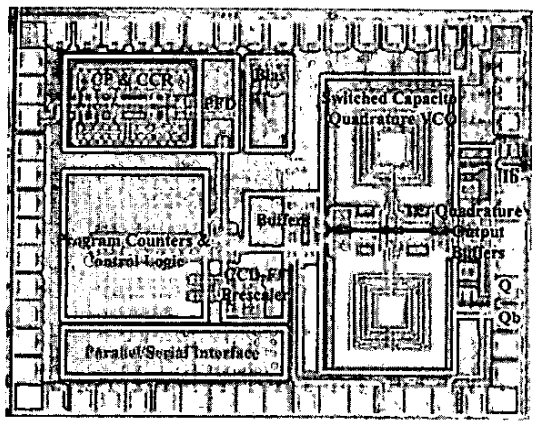


Fig. 9. Die photograph

IV. CONCLUSION

We present the design and implementation of the frequency synthesizer with the integrated quadrature VCO, a prescaler using the complementary clocking dynamic flip-flop, and the PFD using the charge pump current sensing scheme. The designed prescaler has not only low power consumption but also maximum operating frequency of 5.1GHz. Also, the dead-zone free PFD/CP scheme automatically detects the minimum delay for the PFD reset irrespective of parasitic effects and thus generates minimum reference spur.

Table 1. Summary of the measured frequency synthesizer

Technology	0.18um Triple-Well CMOS
Frequency Range	1.55 GHz ~ 1.8 GHz
Frequency Output	Quadrature (I / Ib / Q / Qb)
Max. VCO Phase Noise	-140dBc@8MHz
F_{REF}	5MHz
Loop Filter Bandwidth (f_p)	~100kHz
In-Band Phase Noise	-82dBc@10kHz
Reference Spur Level	<-120dBc
Locking Time	~35us (40MHz jump)
Power Supply	VCO/Buffers/CP/PFD:1.8V Counters/Interface/Prescaer: 1.8V
Current Consumption	$VCO/Buffer_{Prescaler}$: 5mA
	PFD/CP/Counters/Interface/Presc aler: 2.5mA
Area	2000 x 1500 um^2

The frequency synthesizer has been fabricated in a single-poly, six-metal, triple-well CMOS 0.18μm technology. The measured spur is too small to be depicted. The total power consumption of the frequency synthesizer is about 7.5mA. Fig. 9 shows the die photograph, and the chip area is 2000 x 1500 um^2. The overall measured performances are summarized in table 1.

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